AN1690
APPLICATION NOTE

FAILSAFE BIASING FOR ST485

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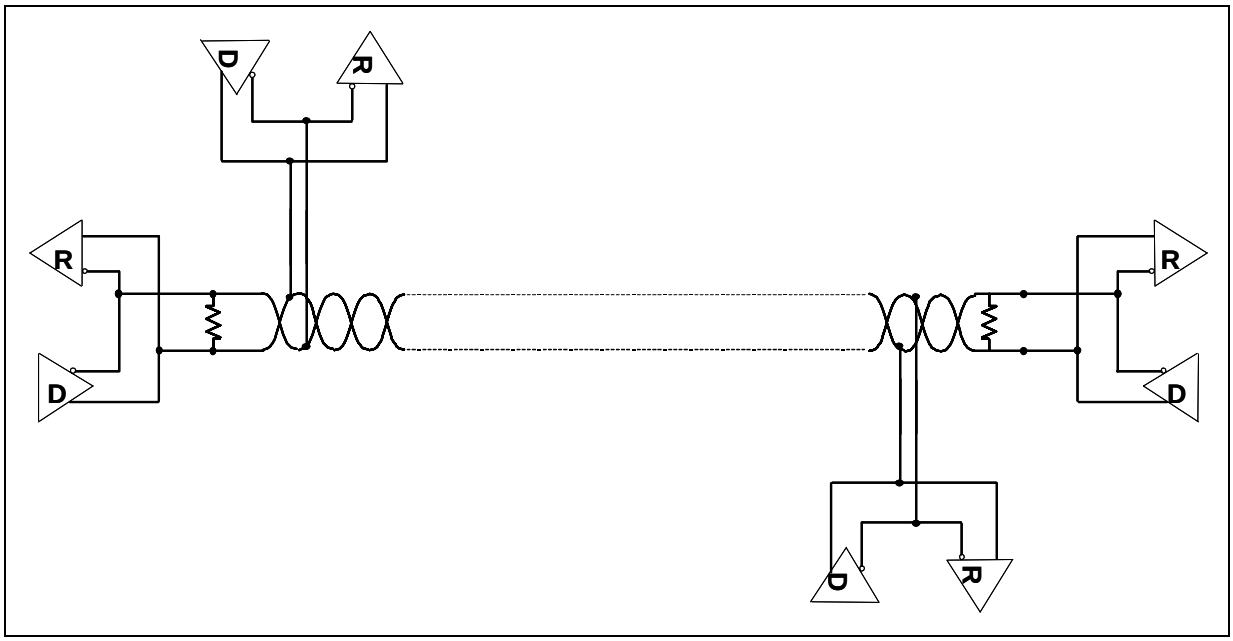
1. ABSTRACT

ST485 is an RS-485 based interface designed for multipoint differential transmission on a single twisted pair cable. It allows half duplex bi-directional transmission, long cable lengths and high data rates.
Typical applications include LANs, industrial (PLC devices), automotive and computer interfaces.
The system evolution in the data communication field leads to the development of faster devices with lower data bit error rate. The ST485 meets all these requirements. Fig.1 shows a typical multipoint bus configuration.

Figure 1: Typical RS485 line



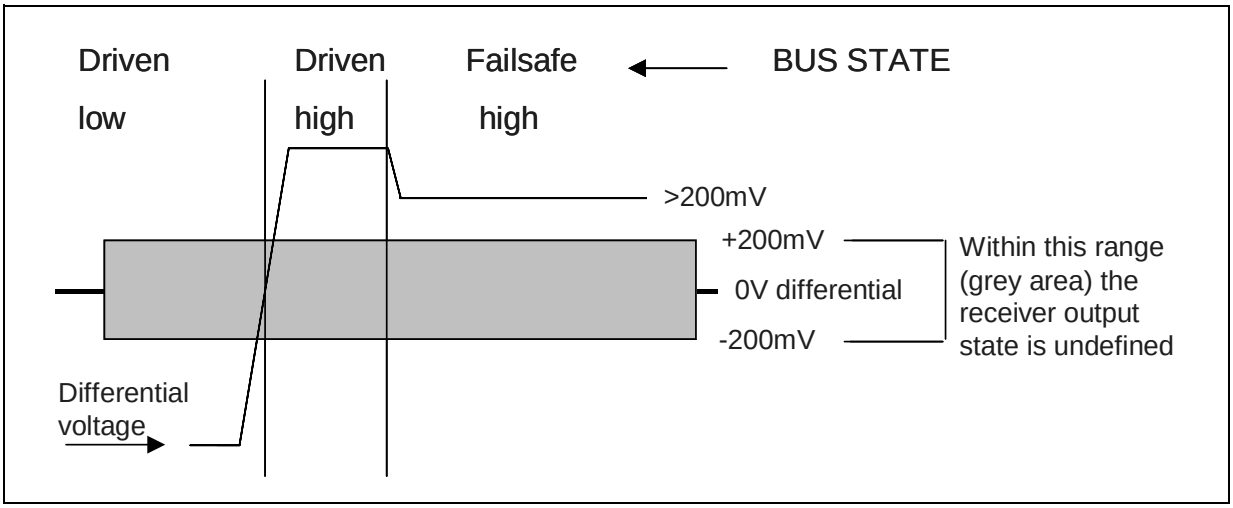
2. OVERVIEW

In a point-to-point configuration (such as the RS-422 standard) the driver is normally always enabled. Therefore the bus can remain only in the HIGH or LOW state (the bus is always biased). In a multipoint application, when more than one driver is physically connected to the bus and only one driver at a time is enabled during data transmission, all the drivers can be disabled when there is no data to send. In this case there is no bus biasing (undefined state). Failsafe biasing solves this problem providing the bus with a proper known state. This application note describes the topic of failsafe biasing.

3. BUS STATES

When a bus is driven by an active driver, it can be in one of two states, either high or low. It can also be kept in one of these states by external pull-up resistors that provide the necessary voltage to get a known bus state. The undefined state in RS-485 standard buses occurs every time the differential voltage is less than +/-200mV. In fig. 2 the bus is driven from low to high and is then disabled. The bus, however, remains high due to external failsafe biasing.

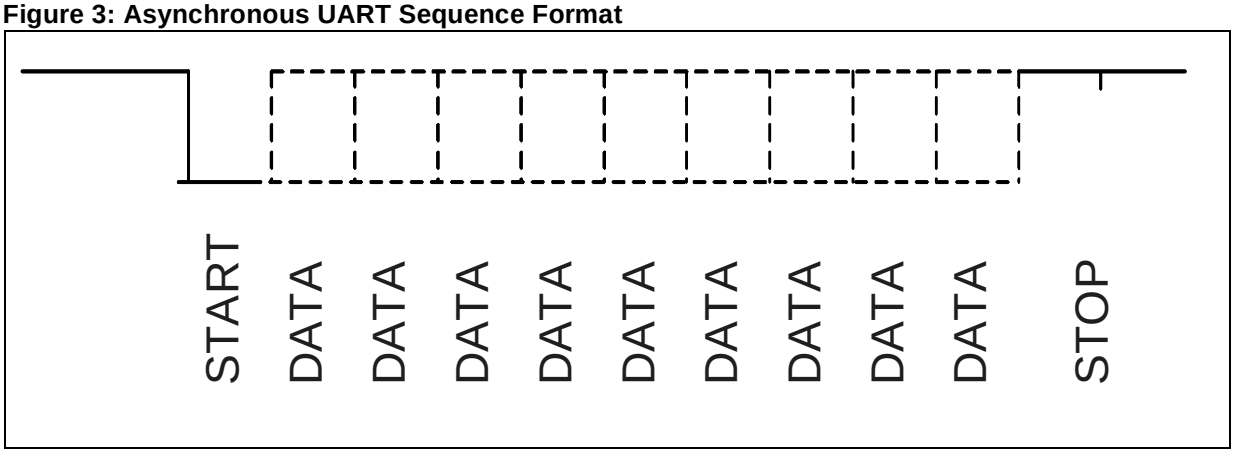
Figure 2: Differential Plot for Driver Outputs



4. DATA TRANSMISSION PROTOCOL

One of the most well known formats for low speed data transmission is the UART timing format. It is an asynchronous protocol, typically composed of 12 bits. The timing sequence starts with a transition from high to low. Next there are 9 data bits (8 data bits plus a parity bit). Finally, the line remains high for one or two bits, which represent the end of the character.

Figure 3: Asynchronous UART Sequence Format



In a multipoint application, when no more data has to be sent, the line should remain high until the next start bit, but since the active driver is disabled, and all other drivers are off, this is not easy to achieve. One way to solve this problem is the use of an alternate protocol (software solution). The other way is to use failsafe biasing (hardware solution).

5. INTERNAL FAILSAFE AND BUS TERMINATION

Transceiver manufacturers avoid external biasing resistors by providing internal pull-up resistors at the receiver inputs, which is effective for detecting open circuits or for those applications where termination resistors are not needed. The line termination resistors (typically 54~120ohms for a twisted pair cable) load the line avoiding the need for internal pull-up resistors to define the receiver output. Fig. 4 shows differential voltage levels for different line conditions for the ST485 receiver interface. Note: there is no driver leading the line.

Figure 4a: Terminated Line (on both sides)

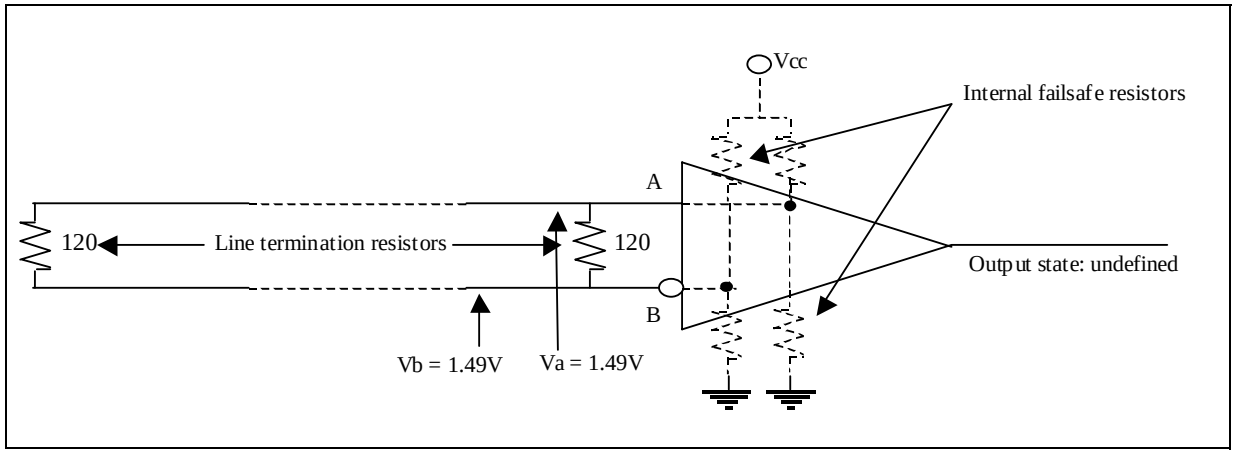


Figure 4b: Open Terminated Line (end side only)

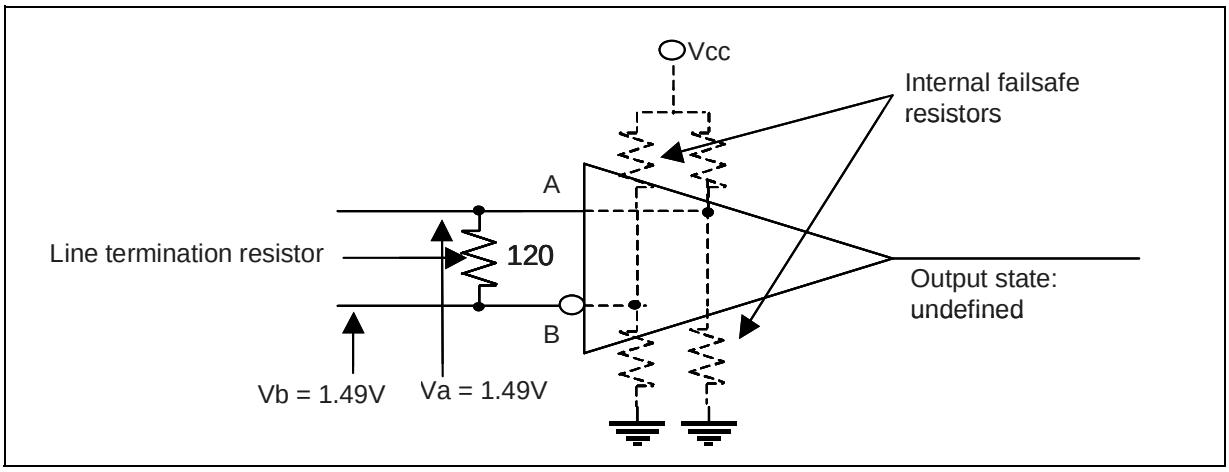
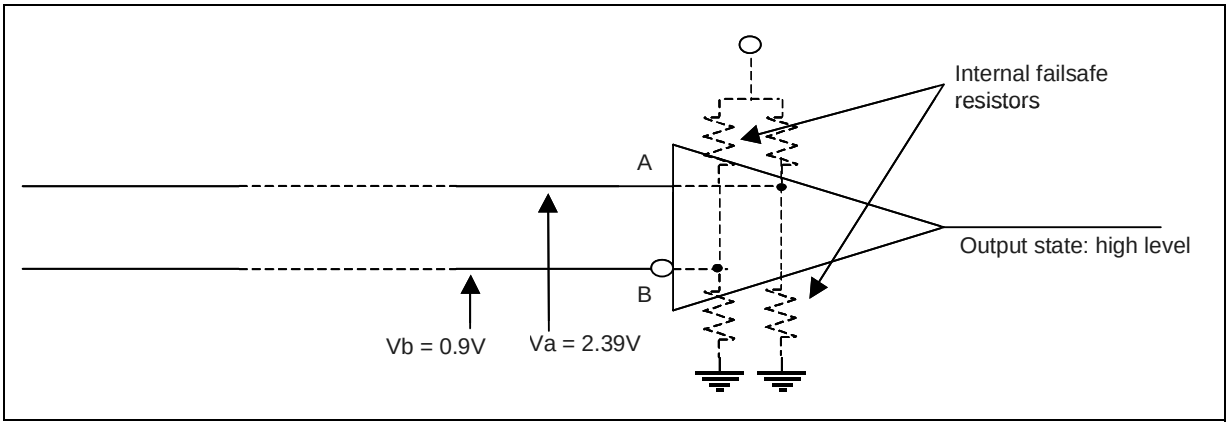


Figure 4c: Unterminated or Open Line

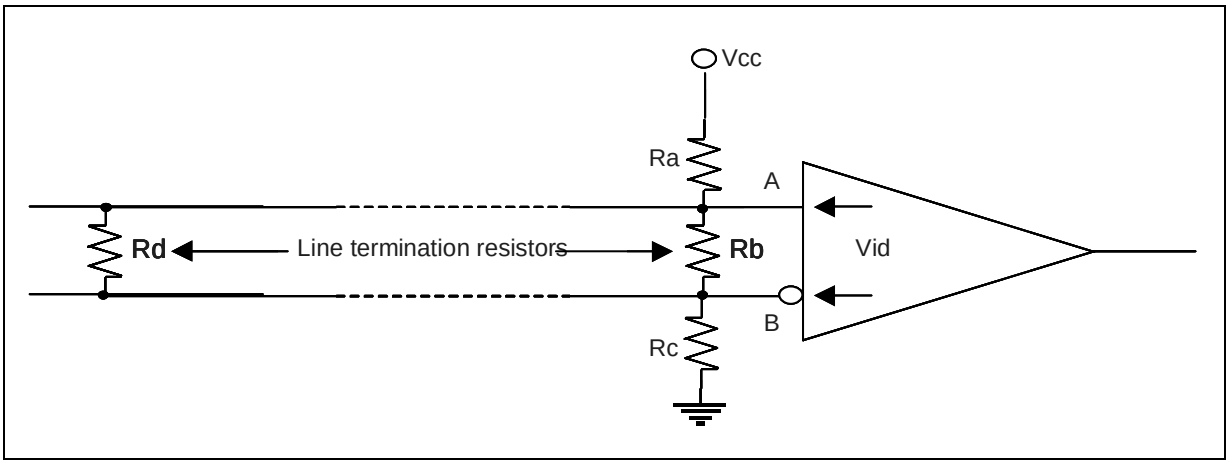


6. DC TERMINATED FAILSAFE RESISTOR VALUE CALCULATIONS

The external resistors are selected so that they provide at least a 200 mV bias across the line, without excessively loading the active driver. In addition, some other conditions should be met:

- The pull-up (Ra) and pull-down (Rc) resistors should be of equal value in order to load the driver outputs symmetrically.
- Termination resistor (Rd) should match the characteristic impedance (Zo) of the line cable, in order to avoid signal reflections.
- At the other end of the cable, the equivalent resistance of Ra, Rb, and Rc should also match the characteristic impedance of the line. In the following fig. 5, the equivalent resistance is Rb//(Ra+Rc), that means Rb must be greater than Zo and Rd.

Figure 5: External Failsafe and Line DC Termination Resistors



The failsafe bias Vid is the voltage drop across the line. Therefore, the failsafe bias is simply a voltage divider between Rb//Rd, Ra and Rc. Note that this formula neglects cable resistance, and that Rb is in parallel with Rd (Rb//Rd).
The choice of resistors must take into account other factors such as power supply voltage tolerance and resistor tolerance, so that under worst case conditions, Vid is greater than 200mV.

7. EXAMPLE CALCULATION FOR THE SCHEMATIC IN FIGURE 5

For this example we assume that the cable has a characteristic impedance Zo=120 ohms and that the power supply voltage Vcc is 5V. We also assume that Rb and Rd are equal and their value matches Zo (Rb=Rd=Zo=120 ohms).

- Calculate the equivalent resistance of Rb//Rd. Rt = 120//120 = 60 ohms.
- Calculate Ra and Rc for a Vid = 200mV.
  - Vid = Vcc (Rt/(Rt+Ra+Rc)). Solving for Ra+Rc
  - Ra+Rc = ((Vcc)Rt/Vid)-Rt. Ra+Rc = ((5V)60ohm/0.2V)-60ohm = 1440 ohm.
  - Ra = Rc = 720ohm
- Recalculate the equivalent termination resistance at the end of the cable. Req = Rb//(Ra+Rc).

Rb = 120//(720+720) = 110 ohm. This value is close (<10%) to the characteristic impedance Zo. However Req could be matched to Zo by setting the following equation:

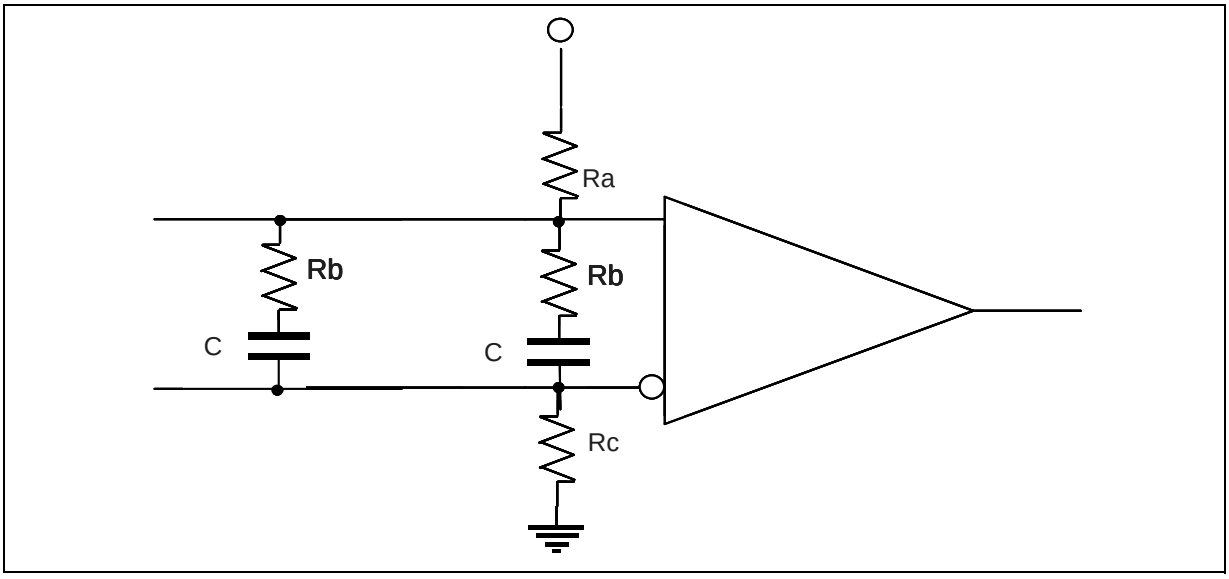
Zo = Rb//(Ra+Rc); then Rb = 131 ohm

- The calculated values for Ra and Rc could be slightly decreased to provide a Vid >200mV, and to meet the worst case power supply and resistor tolerance conditions. Then Ra and Rc could be 500 ohm. However the value of Ra and Rc should not be reduced too low in order to minimize the driver loading when the driver is active. An active driver is required to create a minimum of 1.5V across the cable termination. The use of low resistance pull resistors makes this voltage more difficult to meet.

8. AC TERMINATED FAILSAFE RESISTOR

The DC termination (with and without failsafe biasing) increases power consumption due to the current flow through the termination resistors. In order to reduce the current absorbtion, the failsafe network could be modified as shown in figure 6.

Figure 6: AC Termination with External Failsafe



The RC termination blocks DC current. The value of Ra and Rc can be increased, but not so much that noise immunity is made worse.
Although Rb always equals the cable's characteristic impedance (Zo), the choice of C requires some judgement. Large C values provide good terminations by allowing any signal to see an Rb that matches Zo, but large values also increase the driver's peak output current and the time constant RC, therefore decreasing signal quality.

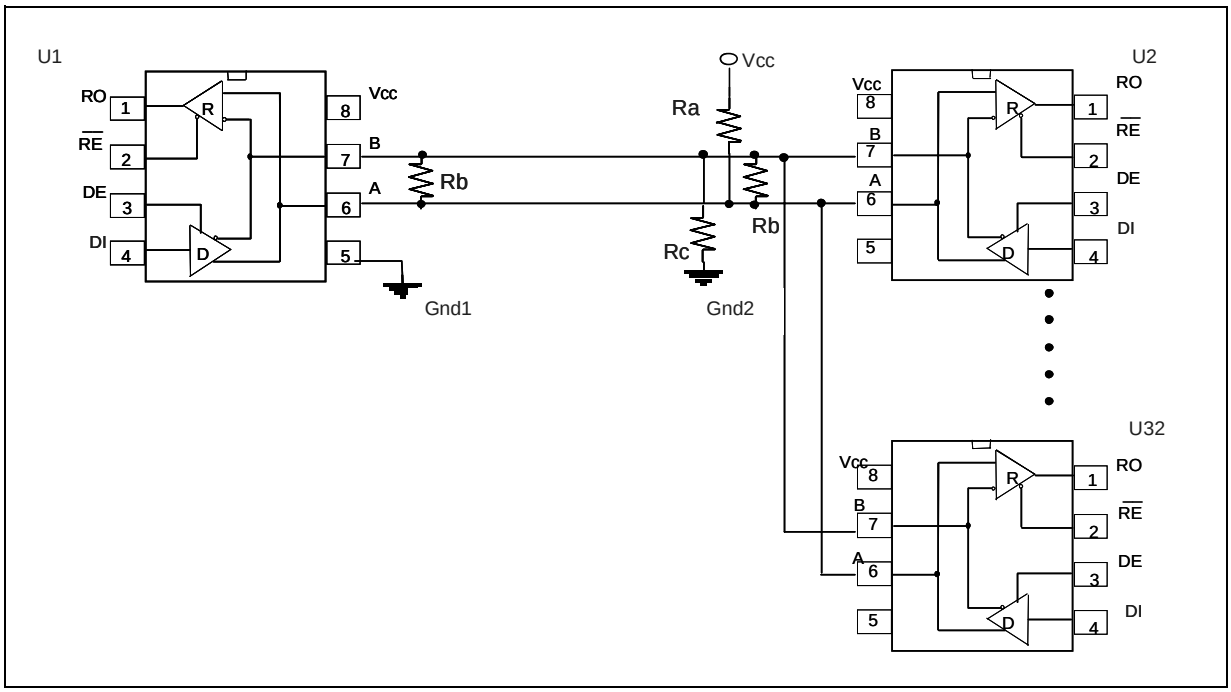
9. FAILSAFE IN MULTIPOINT TRANSMISSION BUSES

As discussed in the example of the calculation for failsafe resistors, when calculating their values, the following conditions must be satisfied:

- The driver must be able to develop a differential output voltage Vod >=1.5V

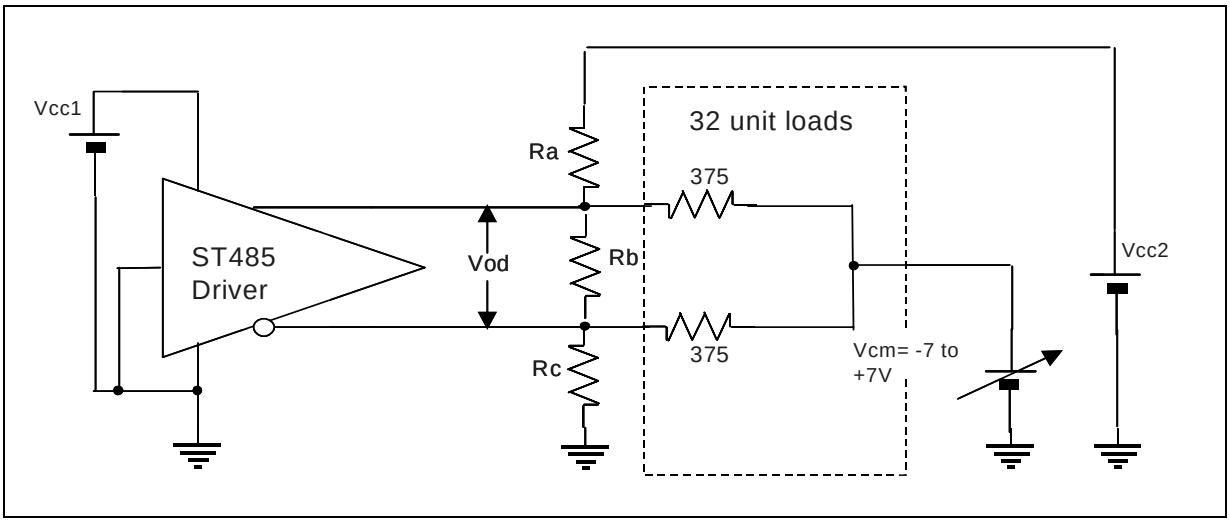
The excessively low resistance of the pull resistors could affect the driver differential output voltage. In a multipoint application, where up to 32 transceivers could be connected in parallel to the transmission line (fig. 7), the differential output voltage drops, due to the equivalent input impedance of all the receivers connected. A minimum input impedance of 12 kohm for each receiver is required, so in the worst case of a fully loaded network (32 unit loads) the equivalent resistance seen by the active driver is (12 kohm / 32) = 375 ohm.

Figure 7: Multipoint Transmission Line with ST485



This value should be reduced in order to take into account that there are 31 drivers in a high impedance state, each with a leakage current. However in the ST485 device this current is less than 10uA, so its effect can be neglected. With regard to the ground shift, the previous schematic can be modelled as shown in fig. 8, in order to verify the driver output voltage capability.

Figure 8: Equivalent Test Circuit for a Fully Loaded Network



This test was performed on the ST485 driver. The resistor values were:
- Ra = Rc = 500 ohm
- Rb = 60 ohm

With the common mode voltage Vcm varied from -7 to +7V, the device meets the 1.5V minimum differential voltage (Vod).

10. FAILSAFE CIRCUIT COMPARISONS WITH ST485

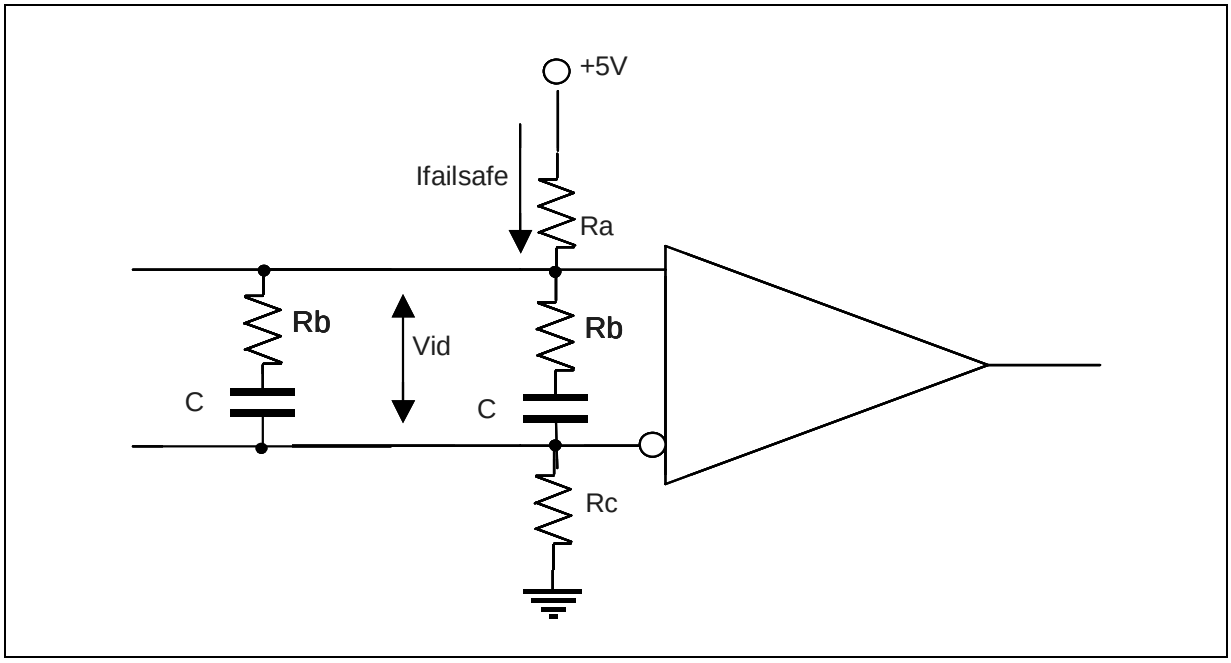
The following measurements were performed with two ST485 devices connected in point-to-point configuration across a twisted pair cable of 1m length. The following table summarizes the DC characteristics with different termination circuits.

Table 1: DC Failsafe Characteristics

Schematic	Ra = Rc (ohm)	Rb (ohm)	C (nF)	Vid (mV)	Ifailsafe (mA)	Receiver output state
No termination	-	-	-	1430	-	Fixed high (internal failsafe)
DC termination	-	120	-	1.45	-	Undefined
Failsafe DC termination	500	120	-	280	4.72	Fixed high
Failsafe AC termination	22k	120	100	4040	0.0316	Fixed high

Note: Vcc=5V

Figure 9: DC Failsafe Characteristics



Another test was performed to verify the behaviour of the different termination circuits when an AC signal is present on the line. The following pictures show the eye patterns of the signals driven respectively at the end of a 100 m cable, and on the receiver output. The driver was led by means of a PRBS (pseudo-random bit signalling) generator with 5 Mbit/s data rate.

Figure 10: Failsafe DC Termination - Eye pattern and test circuit

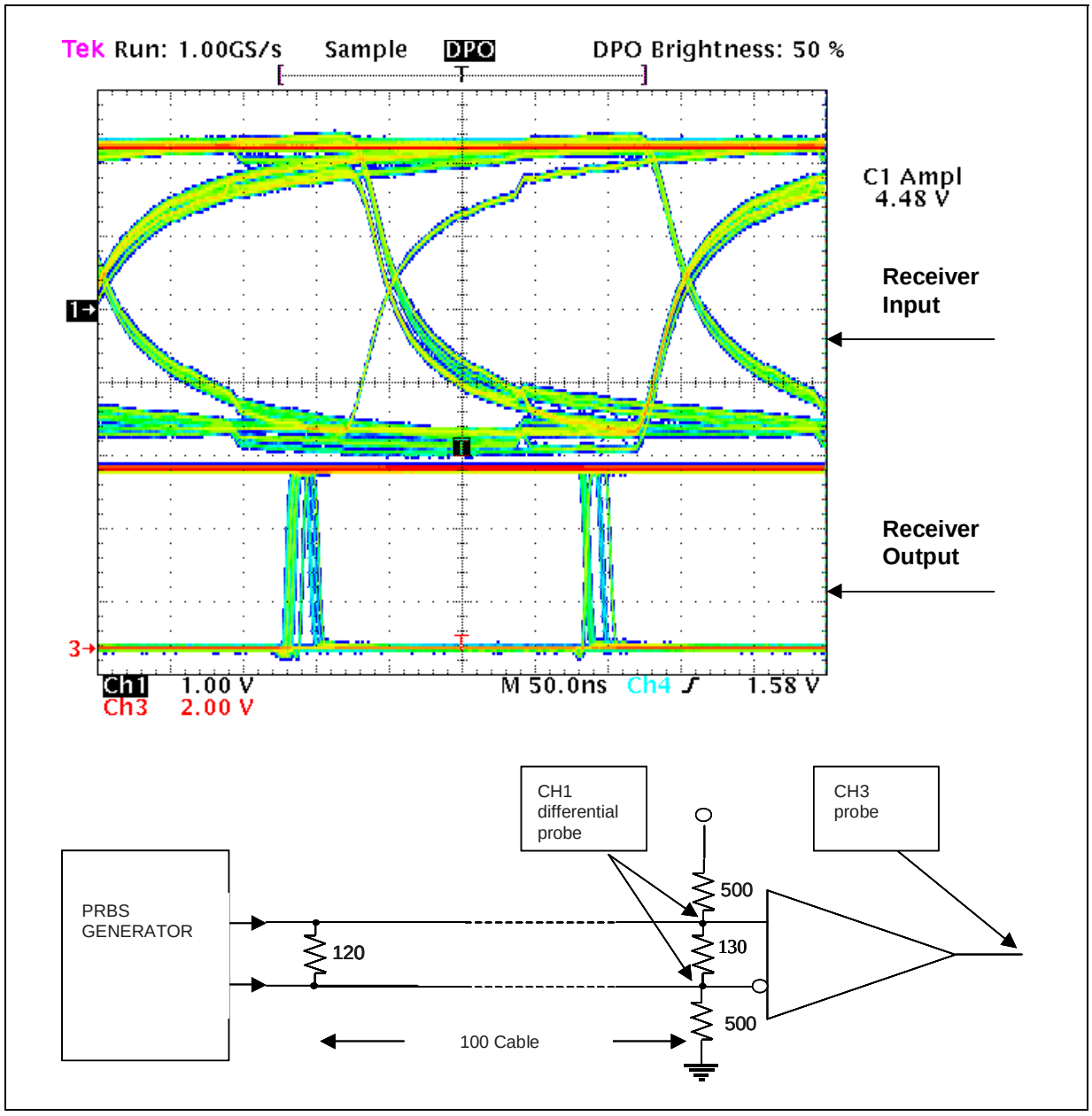


Figure 11: Failsafe AC Termination - Eye pattern and test circuit

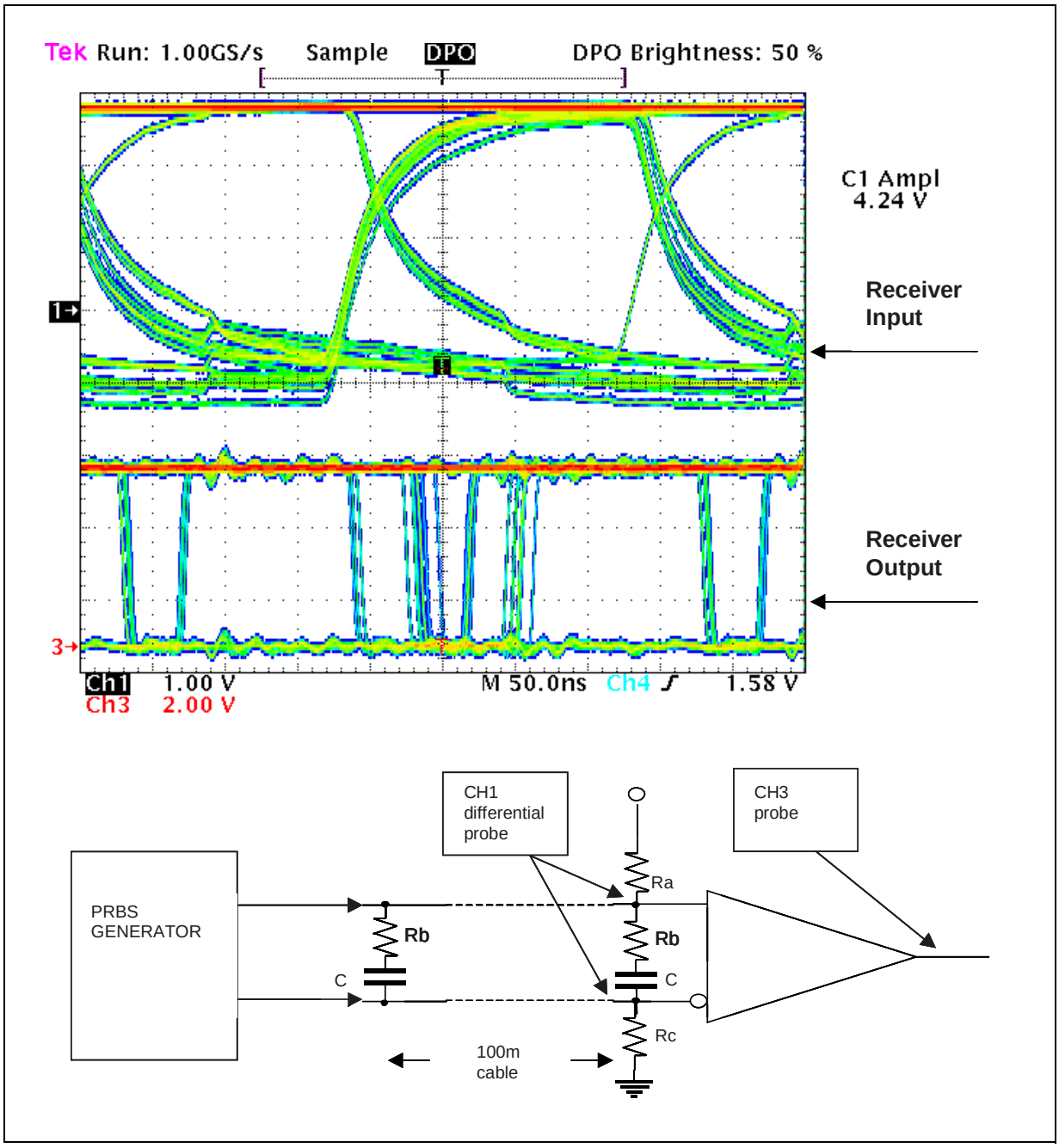


Figure 10 and figure 11 show how the choice of termination could influence the signal quality at the end of the transmission line. In particular, the AC termination seems to be worse than the DC one, when the cable length increases (the output presents jitter and inter-symbolic interferences).

11. CONCLUSION

External failsafe bias resistors can be used to solve the idle line state problem that commonly occurs in multipoint applications using asynchronous protocols. This hardware approach is well accepted. In fact many complete interface standards such as SCSI-1 and 2 (Small Computer System Interface) and IPI (Intelligent peripheral Interface) have adopted this method. This application note provides guidance to select proper failsafe schematic and external component values that will provide an adequate bias, while minimizing the loading effect on the line driver.